Attorney Docket No. B-3964 618029-8

PATENT

AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant : Lap-Wai Chow, et al	)	On Appeal to the Board of Appeals
Patent Application No.: 09/768,904	)	
Filed: 01/24/2001	)	Group Art Unit: 2815
For: "Integrated Circuit Protection ..."	)	Examiner: Nguyen, Joseph H
	)	Date: August 11, 2006

BRIEF ON APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Final rejection, dated December 16, 2005, for the above identified patent application. Appellants submit that this Appeal Brief is being timely filed, since the notice of Appeal was filed on June 15, 2006.

REAL PARTY IN INTEREST

The present application has been assigned to HRL Laboratories, LLC of Malibu, CA.

RELATED APPEALS AND INTERFERENCES

Appellants submit that there are no other prior and pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-20 and 23-24 are currently pending and Claims 21-22 have been canceled without prejudice. Claims 1-20 and 23-24 are the subject of this Appeal and are reproduced in the accompanying Claims appendix.

STATUS OF AMENDMENTS

No Amendment After Final Rejection has been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

The invention described and claimed in the present application relates to semiconductor devices containing metal traces leading to field oxide layers to prevent and/or thwart reverse engineering of the semiconductor device and the process or method for fabricating such devices.

In order to avoid the expenses of designing and developing semiconductor integrated circuits, some developers practice reverse engineering by disassembling products manufactured by somebody else and closely examining them to determine the physical structure of the integrated circuits, followed by copying the products. Such practices harm the true developer of the product and impair its competitiveness in the market-place, because the developer had to expend significant resources for the development, while the reverse engineer did not.

Usual practice of reverse engineering is to try to determine a basic structure of an integrated circuit by identifying metal patterns in the higher level metal layers in the circuit. Metals on these layers route the electric signals between circuit blocks. Once a basic circuit function is determined, rather than look at each next transistor pair, the reverse engineer will utilize the similarity in the upper metal patterns and assume each circuit section showing a particular pattern is the same function. Hence, there is a need for a defensive method which can help to provide protection against the reverse engineering of semiconductor circuits.

According to the present disclosure, the reverse engineer is forced to examine nearly every connection of every transistor pair in an integrated circuit which requires a significant amount of time and money thereby making the reverse engineering of the integrated circuit time and cost prohibitive and leading to *de facto* protection against reverse engineering.

A first embodiment of a semiconductor device adapted to prevent and/or thwart reverse engineering and a method for fabricating it according to the present invention is best depicted in Figure 2. The first embodiment according to the present invention is exemplified in Claims 1-8 and 17-18.

A second embodiment of a semiconductor device adapted to prevent and/or thwart reverse engineering and a method for fabricating it according to the present invention is best depicted in Figure 3. The second embodiment according to the present invention is exemplified in Claims 9-16, 19-20 and 23-24.

Referring to Figures 1 and 1(b), the semiconductor devices contain transistors that typically comprise a source 1, a drain 2, a gate 3 and field oxide layers 4. The semiconductor devices may further contain metallization 10 that is connected to the source 1 or drain 2 of the transistor though a metal plug 7. Typically, the reverse engineer looking at the metal plug 7 assumes that metallization 10 connected to the metal plug 7 is connected to either source 1 or drain 2 and determines the functionality of the semiconductor device based on that connection. Referring to Figure 2, in the first embodiment, by providing metal plugs 7 that are not electrically connected to either source 1 or drain 2 of the transistor (i.e. contact region 12), the reverse engineer would wrongfully conclude that there is a connection to the contact region 12, which would lead to the wrong conclusion as to the functionality of the semiconductor device. This may be accomplished by disposing a metal plug 7 above a field oxide layer 11 that is disposed within the contact region 12 and electrically isolates the metal plug 7 from the contact region 12, as disclosed in the first embodiment of the present invention. See Figure 2 of the specification.

Referring to Figure 3, in the second embodiment, by providing metal plugs 7 that are not electrically connected to either source 1 or drain 2 of the transistor (i.e. contact region 9), the reverse engineer would also wrongfully conclude that there is a connection to the contact region 9, which would lead to the wrong conclusion as to the functionality of the semiconductor device. This may be accomplished by disposing a metal plug 7 above a field oxide layer 4 that is disposed next to the contact region 9, as

disclosed in the second embodiment of the present invention. See Figure 3 of the specification.

In summary, referring to Figures 2-3, by utilizing metal plugs 7 that are not electrically connected to the contact regions 12 and 9 of the transistor, the present invention is intended to prevent and/or thwart reverse engineering of the semiconductor devices by forcing the potential reverse engineer to examine every metallization 10 within the semiconductor device, which would require much time and money there by making the reverse engineering of the integrated circuit cost and time prohibitive.

Overview of independent Claims 1, 5, 9 and 13

The embodiment of a semiconductor device adapted to prevent and/or thwart reverse engineering and a method of for fabricating it is exemplified in independent Claims 1, 5 9 and 13.

Claim 1 of the present disclosure is directed to a semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising: (a) a field oxide layer (11) disposed on a semiconductor substrate and within a contact region (12); (b) a metal plug contact (7) disposed within said contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer, and wherein said field oxide layer electrically isolates said metal plug contact from said contact region; and (c) a metal (10) connected to said metal plug contact. (p. 9, last two lines to p. 10, 1. 16; Fig. 2)

Claim 5 of the present disclosure is directed to a method for preventing and/or thwarting reverse engineering, comprising: (a) providing a field oxide layer (11) disposed on a semiconductor substrate and within a contact region (12); (b) providing a metal plug contact (7) disposed within said contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer, and wherein said field oxide layer electrically isolates said metal plug contact from said contact region; and (c) connecting a metal (10) to said metal plug contact. (p. 9, last two lines to p. 10, 1. 16; Fig. 2)

Claim 9 of the present disclosure is directed to a semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising: (a) a field oxide layer (4) disposed on a semiconductor substrate adjacent a contact region (9); (b) a metal plug contact (7) having a first surface and a second surface opposite said first surface, said metal plug contact disposed outside said contact region, wherein said second surface of said metal plug contact is disposed above said field oxide layer and in contact with a dielectric material, wherein said metal plug contact is electrically isolated from said contact region; and (c) a metal connected to said first surface of said metal plug contact. (p. 10, last three lines to page 11, l. 7; Fig. 3)

Claim 13 of the present disclosure is directed to a method for preventing and/or thwarting reverse engineering, comprising: (a) providing a field oxide layer (4) disposed on a semiconductor substrate adjacent a contact region (9); (b) providing a metal plug contact (7) having a first surface and a second surface opposite said first surface, said metal plug contact disposed outside said contact region, wherein said second surface of said metal plug contact is disposed above said field oxide layer and in contact with a dielectric material, wherein said metal plug contact is electrically isolated from said contact region; and (c) connecting a metal to said first surface of said metal plug contact. (p. 10, last three lines to page 11, l. 7; Fig. 3)

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Issue 1: Whether Claims 1-3, 5-7, 9-11, 13-15, 17-20 and 23-24 are patentable under 35 U.S.C. 102(b) in view of Sun, U.S. Patent No. 5,345,105, (hereinafter "Sun")?

Issue 2: Whether Claims 4, 8, 12 and 16 are patentable under 35 U.S.C. 103(a) in view of Sun and further in view of Liu, U.S. Patent No. 6,165,861, (hereinafter "Liu")?

ARGUMENT

Issue 1: Whether Claims 1-3, 5-7, 9-11, 13-15, 17-20 and 23-24 are patentable under 35 U.S.C. 102(b) in view of Sun, U.S. Patent No. 5,345,105, (hereinafter "Sun")?

In the final Office Action of December 16, 2005, the Examiner rejects Claims 1-3, 5-7, 9-11, 13-15, 17-20 and 23-24 under 35 U.S.C. 102(e) as being anticipated by Sun. Appellants respectfully disagree with the Examiner's rejection for the following reasons and request that the rejection be reversed on appeal.

Claim 1

The Examiner asserts that Sun discloses, "on Figure 6 of Sun a semiconducting device adapted to prevent and/or to thwart reverse engineering..." (See Page 2 of the Official Action.)

The Examiner also asserts that "Sun et al. does not teach reverse engineering prevention...." (See Page 2, last paragraph, of the Official Action.)

Appellants are at a loss as to what the Examiner is trying to assert. Either the Examiner is asserting that Sun, et al. does disclose a device adapted to prevent and/or thwart reverse engineering **or** does not disclose a device that prevents and/or thwarts reverse engineering. The Examiner is **not entitled** to take one position in one part of the Official Action, and then a completely different position in another part of the Official Action.

Moreover, if the Examiner does believe that Sun discloses "a semiconducting device adapted to, prevent and/or thwart reverse engineering" as asserted on Page 2 of the Official Action, it is noted, with all due respect to the Examiner, that Sun does not appear to use the word "reverse" or "engineering" at any place in the disclosure. As such, the Examiner apparently has no possible basis in making the assertion noted above.

The assertion made by the Examiner is undoubtedly a factual assertion. Although the Examiner was requested to put the assertions into affidavit format as specifically

required by the Rules of Practice, see 37 C.F.R. §1.104(2)(d), the Examiner failed to do so. Since the Examiner has not complied with the Rules of Practice, the factual assertion being made by the Examiner must be ignored.

On the issue of the weight to be given to the terms "adapted", the Examiner cites In re Hutchinson, 69 USPQ 138, without even paying the Appellants the courtesy of noting that the Examiner is relying on mere dicta.

Appeal Board's attention is directed to the MPEP, which does address "adapted to" terminology in §2106 and §2111.04. Note is made of the fact that the MPEP §2106 and §2111.04 do not cite In re Hutchinson, which makes it clear that the Commissioner does not put much credence in the dicta set forth in Hutchinson. Appellants object to the Examiner's reliance on the dicta. Note is also made of the language of the MPEP where the use of that language only may "raise a question" as to the limiting effect of the language. The MPEP does not sanction that which the Examiner is doing in this Application where the Examiner is ignoring the "adapted to" terminology almost seemingly out of hand.

The Examiner states that the "adapted to" language "only requires the ability to so perform." Is the Examiner saying that with respect to Appellants' disclosure or to the prior art? Or is the Examiner is trying to state that only the Appellants' disclosure needs to have the "ability to so perform" and the prior art does not require "the ability to so perform"? If so, then the Examiner is basically asserting that the prior art does not need to meet each and every limitation of the claim even though the Examiner sets forth the rejection under 35 U.S.C. §102(b). That is obviously improper and should be reversed on appeal.

On the other side of the coin, if the prior art needs to possess "the ability to so perform," to use the language of the Examiner, then how does Sun possibly possess the ability to "prevent and/or thwart reverse engineering", particularly when Sun does not teach reverse engineering prevention as admitted by the Examiner in the Official Action?

Next, Appellants assert that the "contact region" feature of Claim 1 is not met by Sun. The Examiner asserts that the term "contact region" as recited in Claim 1 is a broad limitation and the Examiner seems to allege that the Examiner can read it on whatever structures he wants to in Sun. The Appellants believe that this is not the state of the law.

According to the Examiner, the "contact region" recited in Claim 1 is allegedly disclosed by a left side of a Sun's device "10" identified by reference letter "A" added for clarity in Sun's Figure 6 reproduced below.

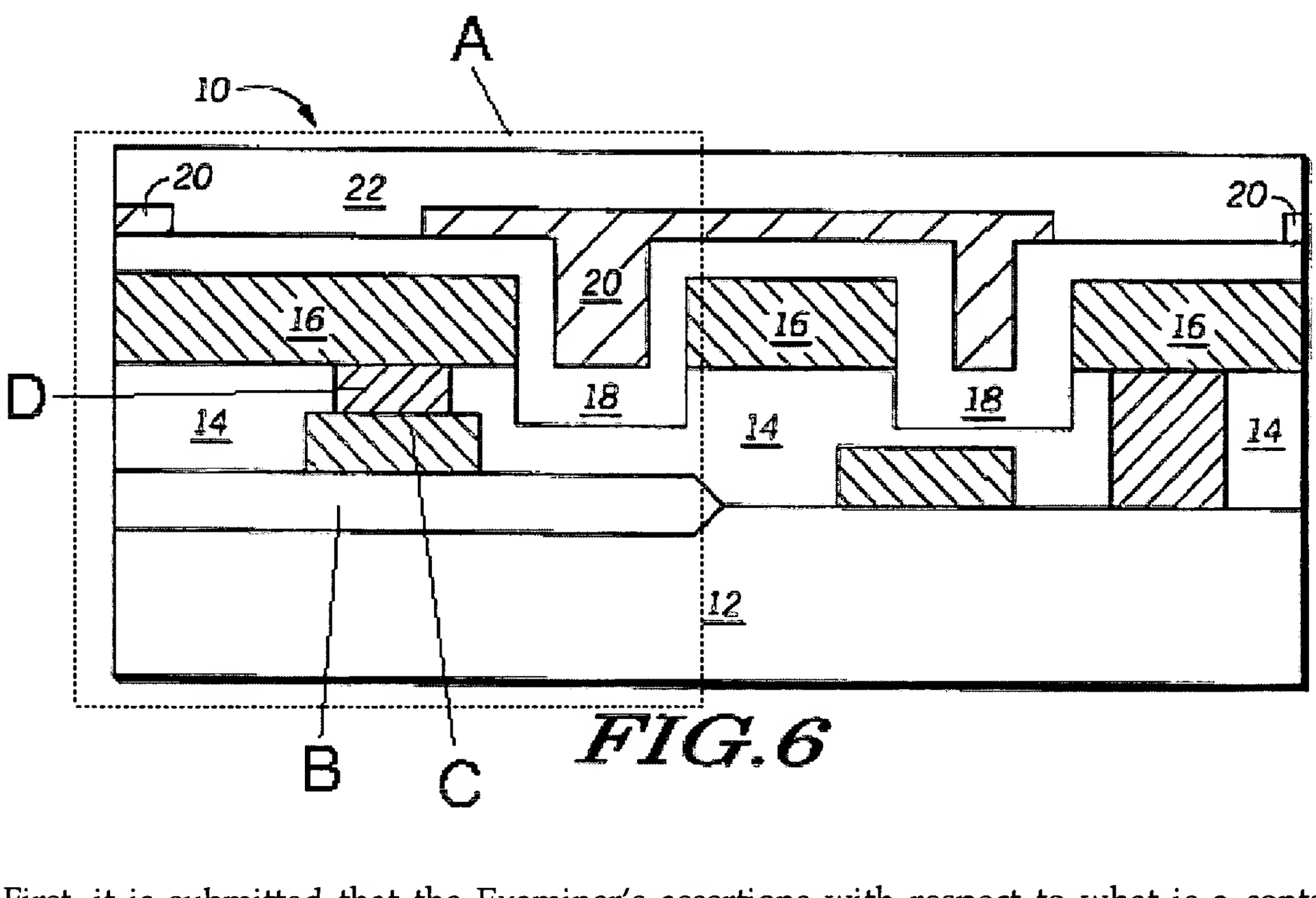

FIG.6

First, it is submitted that the Examiner's assertions with respect to what is a contact region in Sun flies in the face of how the term contact is defined in this art. Enclosed in the Evidence Appendix are pages from "Fundamentals of Semiconductor Processing & Technology" by Badih El-Kareh published in 1995 by Kluwer Academic Publishers. It is noted that contacts are defined by openings, which are formed in the isolation shown on Figure 8.15 of El-Kareh. Note the similarity in the shape of the isolations in Figure 8.15 of El-Kareh and in Figure 6 of Sun, et al, but the utter lack of opening in the left side

"A" of Sun. Because the Examiner failed to identify any openings in the isolation layer of Figure 6 in Sun, et al. in the region that the Examiner defines as being the "contact region" clearly leads to the conclusion that Sun fails to teach the recited "contact region."

What the Examiner defines as "a contact region" is, in fact, a region having zero contacts. While the term "contact region" might be a broad limitation, as the Examiner asserts, it is submitted that it cannot read on something which has no contact, and that is the something which the Examiner has done in examining this Application. That is improper and the rejection based on such improper reasons should be reversed on appeal.

It is submitted that there is one, and only one reason, that the Examiner characterizes the left-hand side "A" of Figure 6 of Sun is being a contact region, that is the desire to reject the claims in this Application on a nonsense piece of prior art by basically ignoring the limitation in its entirety. That is, with all due respect to the Examiner, highly improper and should be reversed on appeal.

Claim 1 also recites "a metal plug contact" which the Examiner asserts is anticipated by a "conductive layer between metal 16 and field oxide..." shown in Sun's Figure 6 reproduced above. The Examiner is also making the assumption that the layer immediately above semiconductor substrate 12, identified by reference letter "B" for clarity on the left hand side of Figure 6 reproduced above is field oxide. First, it is to be noted that the Examiner's assumption that the shape, shown on the left hand side "A" of Figure 6, appears to be field oxide is not based upon any teaching in Sun, but on the information the Examiner apparently knows from prior art. It is noted, with all due respect to the Examiner, that Sun does not appear to use the words "field oxide" anywhere in Sun's application. The point of this observation is that the Examiner's rejection is really not proper under 35 U.S.C. §102, since the Examiner is really saying that it would be obvious to make the layer above the substrate on the left hand side of Figure 1 out of field oxide, meaning that the Examiner is really making an obviousness rejection under 35 U.S.C. §103 as opposed to an anticipation rejection under 35 U.S.C. §102.

Of more import are the two unlabeled cross-hatched boxes identified by reference letters "C" and "D," added for clarity, above the layer "B." The Examiner characterizes those two boxes as "metal plug contact" in making the rejection.

However, in Sun's disclosure, those and the other unnumbered layers are characterized much differently. Appeals Boards' attention is directed to Paragraph beginning at the top of Column 3 of Sun wherein Sun teaches the reader that the "unmarked layers lie adjacent or under dielectric layer 14 and illustrate the fact that dielectric layer 14 could be physically removed or in contact with substrate 12. The unmarked layers are not labeled due to the fact that the unmarked layers are not required in order to understand the invention to disclose herein." It is submitted that the sum and substance of that disclosure is that those unmarked layers are unimportant to Sun's teaching of how to shield a conductor. They appear to be randomly positioned in Sun with no rhyme or reason. The simple reason for the randomness is that they are depicted for one and only one purpose and that is to illustrate the fact that "dielectric layer 14 could be physically removed or in contact with substrate 12" or have devices composed of transistor formations, dielectric layers, conductive formations, etc, be situated between the dielectric layer "14" and the substrate. See column 2, lines 53-68 of Sun. So, although there might be some metal inside those devices, there is no suggestion that they are simply metal plugs as suggested by the Examiner. The boxes "C" and "D" are meant to represent more complex structures that may or may not even exist. That is the sole purpose of their depiction.

However, when the Examiner reads Sun, he sees a metal plug in the cross-hatched boxes "C" and "D" of Figure 6. Why is that so? Could it be because the Examiner has had the privilege of reading Appellants' disclosure and now understands why it might be important to dispose a metal plug on top of field oxide? But that understanding does not come from Sun.

Furthermore, where does Sun teach that the two layers "C" and "D" are metal?

Again, the Examiner ignores that which Sun teaches, but tries to read Sun on Appellants' claims without giving due regard that which Sun really teaches. This Examiner is trying to bend Sun's disclosure, much like a nose of wax, for the sole purpose of anticipating Appellants' claims without giving due regard to that which Sun really teaches.

What the Examiner is also doing is converting Sun from a 35 U.S.C. §102 to a 35 U.S.C. §103 piece of prior art without bothering to cite what additional art he is relying upon to modify Sun, nor explaining where the motivation for making the modifications come from. That is improper and should be reversed on appeal.

Additionally, if the two boxes "C" and "D" can be metal layers, then where is the motivation for turning those two layers into metal layers coming from? With all due respect, it is suggested that there one, and only one, place that the Examiner is getting that motivation, and that motivation is coming straight out of Appellants' own disclosure. The Examiner is, in fact, using Appellants' own disclosure against Appellants, and that is unfair.

Claim 1 is not anticipated by Sun and the Examiner's rejection of Claim 1, and the Claims which depend thereon, based upon Sun, is wholly improper and should be revered on appeal.

Claim 9

The Examiner's rejection of Claim 9, based upon Sun, is filled with as many holes as is the Examiner's rejection of Claim 1.

Appellants assert that the "contact region" recited in Claim 9 is also not met by Sun. According to the Examiner, the "contact region" recited in Claim 9 is allegedly disclosed by a right side of a Sun's device "10" identified by reference letter "X" added for clarity in Sun's Figure 6 reproduced below.

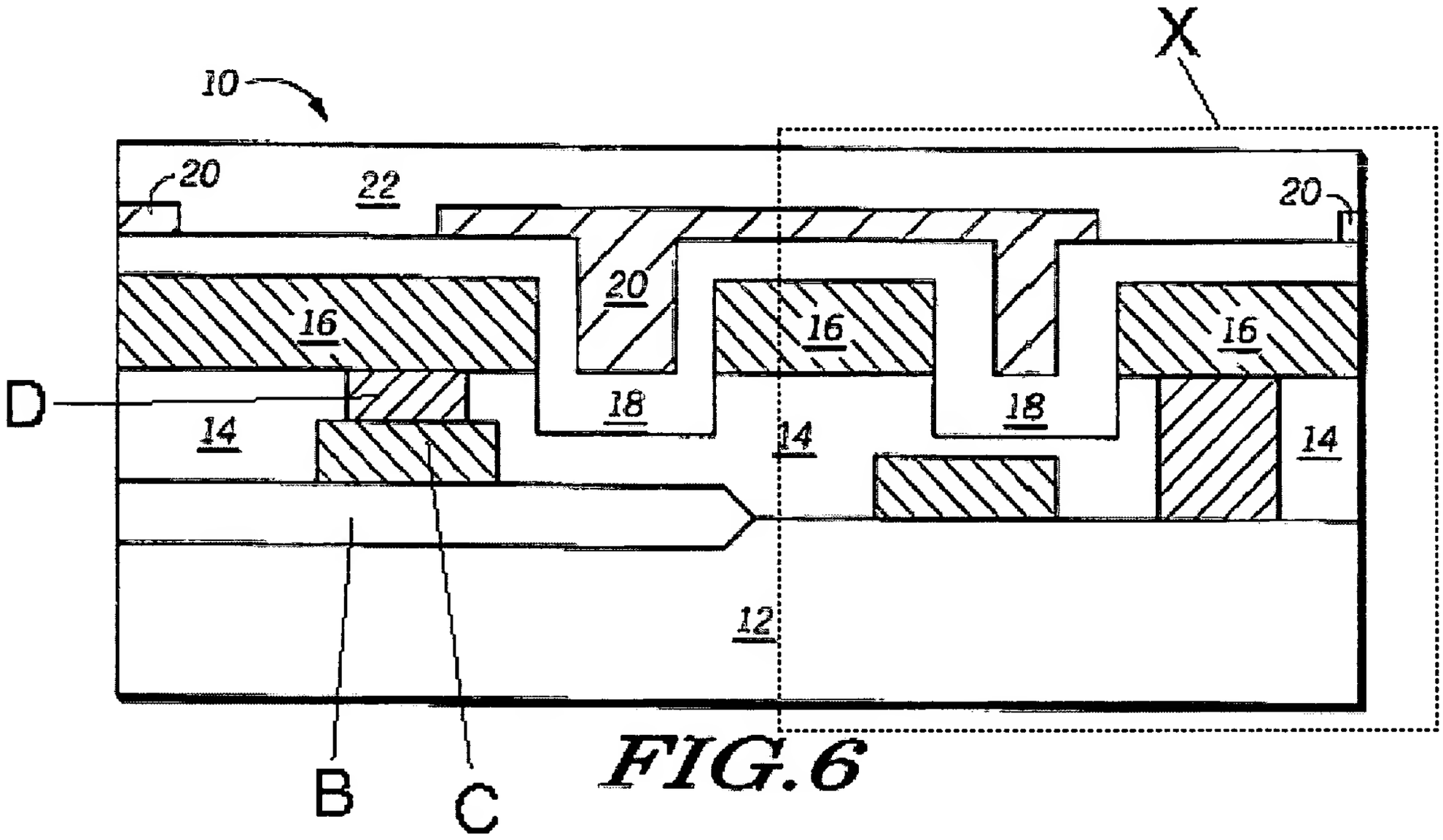

FIG.6

When examining Claim 1, the left hand side "A" of Figure 6 of Sun is characterized by the Examiner as being the contact region. Now, when we come to Claim 9, all of sudden the right hand side "X" of Figure 6 of Sun becomes a contact region. It is just amazing how Sun seems to metamorphise as the Examiner attempts to read Appellants' claims upon it. Just exactly where are the contact regions in Sun? Or is the substrate one big huge contact region? Where does the Examiner see anything like the contacts described by El-Kareh in Sun?

Claim 9 also recites "a metal plug contact" which the Examiner asserts is anticipated by a "conductive layer between metal 16 and field oxide..." shown in Sun's Figure 6 reproduced above. The Examiner is also making the assumption that the layer immediately above semiconductor substrate 12, identified by reference letter "B" for clarity is field oxide.

As stated above for Claim 1, why is the layer "B" characterized as "field oxide" and the two crossed hatched boxes "C" and "D" characterized as being "a metal plug contact" by the Examiner? What possibly makes those two layers "conductive" as asserted by the Examiner in the Official Action?

The Examiner is reading more into Sun than Sun discloses. If the Examiner wants to do that, then the Examiner should have tried converting this rejection under 35 U.S.C. §102 to a rejection under 35 U.S.C. §103 by complying with the Rules of Practice. Where is there any disclosure whatsoever that the two cross hatched boxes on the left hand side of Figure 6 of Sun are either "metal" or "conductive" as asserted by the Examiner?

The Appellants' comments with respect to the "adapted to" terminology in Claim 1 also applies equally well to Claim 9.

The rejection of Claim 9 is improper and should be revered on appeal.

Claim 5

The Examiner rejects Claim 5 without bothering to explain, in any detail, why Claim 5 is being rejected other than to refer the Appellants' attention to the rejection of Claim 1, which is a device claim, while Claim 5 is a method claim.

Claim 5 recites a method of preventing and/or thwarting reverse engineering. The Examiner agrees, in the rejection of Claim 1, that Sun does not teach reverse engineering prevention. If that is the case, then why is Claim 5 allegedly anticipated?

Claim 5 recites, "providing a field oxide layer". The Examiner apparently reads that on the uncrossed hatched layer immediately above layer 12 shown in Figure 6 of Sun. Is not this really an obviousness type rejection as oppose to an anticipation rejection?

Claim 5 also recites, "providing a metal plug contact disposed within said contact region and above said field oxide layer...." The Examiner apparently reads that upon the two cross-hatched boxes shown on the left hand side of Figure 6 between the layer that the Examiner characterizes as being field oxide and layer 16. Where does Sun teach that those layers are metal? As noted above, Sun thinks that those layers are so unimportant that they are not even worth numbering and are apparently randomly drawn merely to demonstrate the fact that Sun's dielectric layer "can be physically removed or in contact with the substrate 12" as specifically taught by Sun.

Why is the region, which is covered by the layer of which the Examiner characterizes as being field oxide in Figure 6 of Sun, characterized as being a "contact region" by the Examiner? Where are the contacts such as those taught by El-Kareh?

It is submitted that the only reason that the Examiner characterizes the left hand side of Figure 6 of Sun as being the contact region and characterizes the two crossed-hatched boxes as being a metal contact is to reject Claim 5. However, the Examiner finds that teaching only in Appellants' own disclosure and then uses it against Appellants in citing Sun since obviously Sun is devoid of any such teaching. Therefore, reversal of the Examiner's rejections is respectfully requested.

Claim 13

Claim 13 is also method claim.

As asked above with respect to Claim 5, how does Sun anticipate a method for preventing and/or thwarting reverse engineering when the Examiner seemingly agrees that Sun teaches no such thing? On what basis does the Examiner assert that the layer, immediately above layer 12 on the left hand side of Figure 6, is a field oxide layer as recited in Claim 13? If Sun is silent as to just what that layer comprises, then the Examiner is characterization of it as being field oxide means that the Examiner is going outside Sun's disclosure to make that assertion. As indicated above, Appellants' request that the Examiner's make all factual assertions in affidavit format as specifically required by the Rules of Practice, see 37 C.F.R. §1.104(d)(2), was not complied with. Hence, the Examiner's factual assertions do not have a proper evidentiary basis and must be ignored.

Furthermore, how do the two crossed hatched boxes shown immediately above the layer, which the Examiner characterized as being field oxide and below layer 16, become a metal plug contact for the purpose of rejecting Claim 13? Where is that disclosed in Sun?

Since Sun does not meet each and every limitation of Claim 13, the rejection under 35 U.S.C. 102 is clearly improper and should be reversed on appeal.

Issue 2: Whether Claims 4, 8, 12 and 16 are patentable under 35 U.S.C. 103(a) in view of Sun and further in view of Liu, U.S. Patent No. 6,165,861, (hereinafter "Liu")?

In the final Office Action of December 16, 2005, the Examiner rejects Claims 4, 8, 12 and 16 under 35 U.S.C. 103(a) as being obvious in view of Sun and Liu. Appellants respectfully disagree with the Examiner's rejection for the following reasons and request that the rejection be reversed on appeal.

Claims 4 and 8

Applicant submits that Claims 4 and 8, at least based on their dependency on Claims 1 and 5, respectively, are believed to be patentable over Sun and Liu, because there is no prima facie 35 USC 103(a) case based on Sun, as shown above, and because the Examiner has not shown where Liu discloses, teaches or suggests the features not found in Sun. Therefore, the Examiner's rejections should be reversed on appeal.

Claims 12 and 16

Applicant submits that Claims 12 and 16, at least based on their dependency on Claims 9 and 13, respectively, are believed to be patentable over Sun and Liu, because there is no prima facie 35 USC 103(a) case based on Sun, as shown above, and because the Examiner has not shown where Liu discloses, teaches or suggests the features not found in Sun. Therefore, the Examiner's rejections should be reversed on appeal.

* * *

Conclusion

For the extensive reasons advanced above, Appellants respectfully contend that each claim is patentable. Therefore, reversal of all rejections and objections is courteously solicited.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this Appeal Brief is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22323-1450 on

August 11, 2006
(Date of Deposit)

Esther M. Hayes
(Name of Person Depositing)

(Signature)

August 11, 2006
(Date)

Respectfully submitted,

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A semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising:

(a) a field oxide layer disposed on a semiconductor substrate and within a contact region;

(b) a metal plug contact disposed within said contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer, and wherein said field oxide layer electrically isolates said metal plug contact from said contact region; and

(c) a metal connected to said metal plug contact.

2. The device as claimed in claim 1, wherein said semiconducting device comprises integrated circuits.

3. The device as claimed in claim 1, wherein said field oxide layer further comprises silicon oxide.

4. The device as claimed in claim 2, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits and bipolar silicon-based integrated circuits.

5. A method for preventing and/or thwarting reverse engineering, comprising:

(a) providing a field oxide layer disposed on a semiconductor substrate and within a contact region;

(b) providing a metal plug contact disposed within said contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer, and wherein said field oxide layer electrically isolates said metal plug contact from said contact region; and

(c) connecting a metal to said metal plug contact.

6. The method as claimed in claim 5, wherein said semiconducting device comprises integrated circuits.

7. The method as claimed in claim 5, wherein said field oxide layer further comprises

silicon oxide.

8. The method as claimed in claim 6, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits.

9. A semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising:
(a) a field oxide layer disposed on a semiconductor substrate adjacent a contact region;
(b) a metal plug contact having a first surface and a second surface opposite said first surface, said metal plug contact disposed outside said contact region, wherein said second surface of said metal plug contact is disposed above said field oxide layer and in contact with a dielectric material, wherein said metal plug contact is electrically isolated from said contact region; and
(c) a metal connected to said first surface of said metal plug contact.

10. The device as claimed in claim 9, wherein said semiconducting device comprises integrated circuits.

11. The device as claimed in claim 9, wherein said field oxide layer further comprises silicon oxide.

12. The device as claimed in claim 10, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits and bipolar silicon-based integrated circuits.

13. A method for preventing and/or thwarting reverse engineering, comprising:
(a) providing a field oxide layer disposed on a semiconductor substrate adjacent a contact region;
(b) providing a metal plug contact having a first surface and a second surface opposite said first surface, said metal plug contact disposed outside said contact region, wherein said second surface of said metal plug contact is disposed above said field oxide layer and in contact with a dielectric material, wherein said metal plug contact is electrically isolated from said contact region; and
(c) connecting a metal to said first surface of said metal plug contact.

14. The method as claimed in claim 13, wherein said semiconducting device comprises integrated circuits.

15. The method as claimed in claim 13, wherein said field oxide layer further comprises silicon oxide.

16. The method as claimed in claim 14, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits.

17. The device as claimed in claim 1, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

18. The method as claimed in claim 5, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

19. The device as claimed in claim 9, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

20. The method as claimed in claim 13, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

21-22 (Canceled)

23. The device of claim 9, wherein said field oxide layer comprises said dielectric material.

24. The method of claim 13, wherein said field oxide layer comprises said dielectric material.

"Fundamentals of Semiconductor Processing & Technology" by Badih El-Kareh published in 1995 by Kluwer Academic Publishers is enclosed herein. The "Fundamentals of Semiconductor Processing & Technology" was entered in the record with the response, dated March 16, 2006, to the final Office Action dated December 16, 2005.

B-2

FUNDAMENTALS OF SEMICONDUCTOR PROCESSING TECHNOLOGY

by

Badih El-Kareh

IBM Corporation

Graphics and Layout: Richard J. Bombard

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several intervals between polishing and determine the time needed to achieve the required polished thickness.

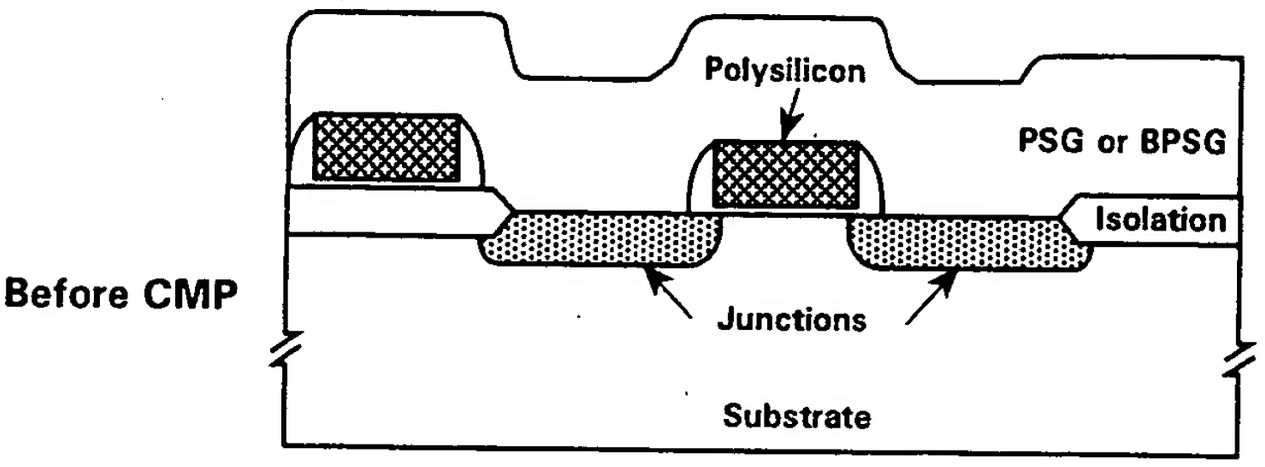

Fig. 8.15 Poly-metal dielectric surface before and after polishing.

8.2.3 Contact Definition

Contacts to silicon or silicide are defined in the insulator using lithography and dry etching techniques discussed in Chaps. 4,5. Dry etching allows the definition of contact openings with high aspect ratio and vertical sidewalls. Since a planar insulator is thinner above polysilicon than above junctions (Fig. 8.15), a sufficiently large etch-rate ratio of insulator to silicon or silicide is required if contacts to both regions are to be etched simultaneously. Alternatively, the substrate surface can be coated with a thin etch-stop, such as silicon nitride, polysilicon, or aluminum oxide, prior to PMD deposition. This allows etching of contact holes to continue to single-crystal silicon without attacking silicide or polysilicon in contacts to the elevated layers. The etch-stop is then removed with an appropriate etchant (Chap. 5). When polysilicon is used as an etch stop, it is important to convert the

film to silicon dioxide by, e.g., high-pressure oxidation after completing the etch process to avoid high leakage between circuits [63]. After etching, contacts must be cleaned to remove any organic material, residual oxide or debris that can cause adhesion problems or block contacts (Chap. 5).

8.3 Metal Interconnects

Metals used in microelectronics must satisfy several requirements to meet the objectives of circuit performance, yield and reliability. They must exhibit low series and contact resistances, negligible penetration into silicon, good adhesion to insulators and contacted surfaces, excellent uniformity, and resistance to corrosion. The metals must also form bondable films that can be delineated into uniform fine-lines of sub-halfmicron widths and spaces, withstand temperature cycling and operating current densities without failure, and be free of contaminants (such as sodium ions). The most common metals used for interconnections and contact fill are aluminum alloys and tungsten. Aluminum meets most of the above requirements but suffers from a failure mechanism at high current densities known as **electromigration,** discussed in Sec. 8.6. Adding small amounts ($\simeq$ 0.5%) of copper to aluminum (or Al-Si) increases the electromigration lifetime. Tungsten is considerably less susceptible to electromigration and can be deposited with greater conformality than physically deposited aluminum. Tungsten, however, exhibits a 2-3 times higher resistivity than aluminum and is typically used in lower-level metals. Copper has also received increased attention because of its higher conductivity and resistance to electromigration than Al. Copper is, however, difficult to delineate and must be "cladded" with a barrier metal to inhibit its diffusion into oxide and silicon where it can cause excessive leakage or shorts [64]. Table 8.4 compares important properties of the three metals.

8.3.1 Metal Deposition

The most widely used techniques to deposit metals are, evaporation, sputtering, and CVD (Chap. 5). Variations to these techniques are collimated sputtering and selective CVD.

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